DRAWING AMENDMENTS

The attached sheet of drawings includes changes to Figs. 1 and 2. This sheet, which includes Figs. 1 and 2, replaces the original sheet including Figs. 1 and 2. In Figs. 1 and 2, the regulator(s) was added.

Please approve the drawing changes that are marked in red on the accompanying "Annotated Sheet Showing Changes" of Figs. 1 and 2. A formal "Replacement Sheet" of amended Figs. 1 and 2 is also enclosed.

Attachments: Replacement Sheet

Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-8 remain in the application. Claims 1 and 4 are subject to examination and claims 2, 3, 5, and 7-8 have been withdrawn from examination. Claims 1 and 4 have been amended.

Applicant herewith affirms election of claims 1-6 directed to a test system for conducting a function test of a semiconductor element on a wafer and the species of Fig. 1. Claims 1 and 4 are generic and are readable on Fig. 1 of the instant drawings.

Under "Drawings" on page 4 of the above-identified Office Action, the drawings are objected to under 37 CFR 1.83(a) because they do not show the regulator of claim 1.

Revised Figs. 1 and 2 of the drawings are enclosed herewith. Figs. 1 and 2 now show the regulator (in Fig. 1) connected between read and supply lines 18, 16 in order to control the potential to be supplied through line 16. Fig. 2 shows respective regulators connected between lines 18 and 16 and 19 and 14. Support for the changes may be found in the original claims and page 4, lines 10-15, page 5, lines 1-8, page 7,

line 17 through page 8, line 2, and page 9, lines 18-21 of the instant specification. No new matter has been added.

In view of the changes the drawings now comply with 37 CFR 1.83(a) and therefore, the Examiner is requested to withdraw the objection.

In the paragraph under "Specification" on page 4 of the above-identified Office action, the Examiner objected to identified portions of the specification because of certain informalities. The Examiner's suggested corrections have been made where appropriate.

Regarding the Examiner's statements relative to the location of the "contact pins" on page 1, line 25 and page 2, line 1, the Examiner is directed to page 12, lines 1-15 for a detailed description of the location of the contact pins.

The Examiner's initial statement that "line 6 should at line 15" is not clear. Therefore, no correction has been made with respect to this statement.

In the paragraph under "Claim Objections" on page 5 of the above-identified Office Action, the Examiner has objected to claims 1 and 4 because of specified informalities. The

Examiner's suggested corrections have been made where appropriate. The Examiner requested a change of "a therminal pad" in lines 16-17 to --the terminal pad--, however, the words "a therminal pad" do not appear in claims 1 or 4. The change suggested in the last sentence has been made in the instant specification.

In view of the changes the Examiner's objections have been obviated and therefore, the Examiner is requested to withdraw the objections to the specification and claims.

In the second paragraph on page 5 of the above-identified Office Action, claims 1 and 4 have been rejected as being anticipated by Hanashey (U.S. Patent 4,023,097) under 35 U.S.C. § 102(b).

The rejection has been noted and the claims have been amended in an effort to even more clearly define the invention of the instant application. Support for the changes is found on page 11, line 23 to page 13, line 16 of the specification of the instant application.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful. Claim 1 calls for, *inter alia*, a test system for conducting a

function test of a semiconductor element on a wafer, the semiconductor element having terminal pads, the test system has:

a pin card having:

a pin card board;

supply contact pins arranged on the pin card board including one of the supply contact pins and another one of the supply contact pins;

a resistance disposed on the pin card board;

a read contact pin disposed on the pin card board and connected to the one of the supply contact pins through the resistance;

the one of the supply contact pins and the read contact pin being configured to contact one of the terminal pads of the element being tested;

the other one of the supply contact pins being configured to contact another one of the terminal pads of the element being tested;

the read contact pin producing a high-impedance electrical read connection to the one of said terminal pads of the element being tested;

the one of said supply contact pins and the other one of the supply contact pins each connected to the voltage source for applying the supply voltage to the one of the terminal pads and the other one of the terminal pads of the semiconductor element being tested; and

a regulator controlling the output voltage based upon an electrical potential of the read contact pin. (emphasis added)

According to the present invention, the test system includes a pin card having a pin card board which carries the supply contact pins and a read contact pin (see page 13, line 13 of the instant specification). A resistance is disposed on the pin card board to connect one of the supply contact pins to the read contact pin. It is important that the resistance is disposed on the pin card board so that the connection between the one of the supply contact pins and the read contact pin is made close to the location where the pin contacts the terminal pads of the wafer.

It is also important that the one of the supply contact pins and the read contact pin both connect to the same terminal pad.

The present invention allows the testing of circuit elements on the semiconductor wafer level (see page 1, line 21 and page 3, line 20 of the instant specification). The semiconductor elements have terminal pads to which the supply and read contact pins are to be connected. The supply and read contact pins may scrape on the terminal pads and may be contaminated with the aluminum material from the pads. This affects the contact resistance between the pin and the terminal pad. Having the resistance on the pin card board means that the resistance is as close as possible to the ends of the pins which contact the terminal pads, thus making it possible to exactly regulate the output voltage to be supplied to the terminal pad (see page 13, lines 8-11 of the instant specification).

It is known in the prior art to have test systems which have a sense and a force line wherein the voltage to be supplied by the force line is controlled from a signal received from the sense line. However, such prior art contacts an integrated circuit through its circuit pins located within the housing of the integrated circuit so that the integrated circuit is in a

state where it is already encapsulated within its housing.

The prior art systems are not optimized in order to contact the terminal pads on the wafer. The present invention solves this problem in that it locates the resistance element within the pin card board so that it is as close as possible to the ends of the contact pins of the test system.

Hanashey discloses a test system with force and sense lines. Hanashey does not disclose that the device under test is on the wafer level. In Hanashey the device under test is already separated from the wafer. Hanashey relates to the testing of an integrated circuit prior to connecting it within the entire manufactured devices, which means within the application system (see column 3, lines 32-33). This means that the integrated circuit to be tested in Hanashey is already housed and is equipped with pins. The test system provides particular input or load to the pins of the integrated circuit (see column 4, line 20; column 4, line 45). Thus, contact to the device under test in Hanashey is made through the pins of the integrated circuit to be tested rather than its terminal pads. A further point is that Hanashey does not clearly disclose whether force and sense line connect to the same terminal of the device so that there is only a loose control of the voltage of the force line.

The problem of contamination of the pins (of the tester) which may result from a scraping of the tester pins on the terminal pads does not exist in Hanashey, since a pin is made of harder material than a terminal pad on the circuit die. Although Hanashey discloses resistors which are in some manner connected between the force and the sense lines (resistors 82, 84, 86 in Figure 1), Hanashey discloses these resistors to be arranged within the core electronics of the tester rather than within the pin card board of the tester.

In the first full paragraph on page 6 of the above-identified Office Action, claims 1 and 4 have been rejected as being anticipated by Swapp (U.S. Patent 5,467,024) under 35 U.S.C. § 102(b).

Swapp discloses another test system having force and sense lines. In Swapp contact is made to the pins of the device under test rather than to its terminal pads (see column 3, lines 64-65). The Examiner refers to resistance 59. However, resistance 59 is a series resistor which is connected serially within line 62. In the present invention, however, resistance 32 is connected between the supply contact pin and the read contact pin. Finally, resistor 49 is not located within the pin card board since the transmission line 62 is still

arranged between resistor 49 and the device under test.

Applicant submits that the present invention improves the concept of sense and force lines for the testing of integrated circuits for a functional test which is reliably performed on the wafer level. The prior art test systems consider only the testing of integrated circuits through the circuit pins which means that the circuits have already been separated into individual devices.

Clearly, the references do not show "supply contact pins arranged on said pin card board including one of said supply contact pins and another one of said supply contact pins; a resistance disposed on said pin card board;
a read contact pin disposed on said pin card board and connected to said one of said supply contact pins through said resistance; said one of said supply contact pins and said read contact pin being configured to contact one of said terminal pads of the element being tested; said other one of said supply contact pins being configured to contact another one of said terminal pads of the element being tested; said read contact pin producing a high-impedance electrical read connection to said one of said terminal pads of the element being tested; said one of said supply contact pins and said other one of said supply contact pins each connected to the

voltage source for applying the supply voltage to said one of said terminal pads and said other one of said terminal pads of said element being tested" as recited in claim 1 of the instant application. Claim 4 contains similar limitations.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1 or claim 4. Claims 1 and 4 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 4.

In view of the foregoing, reconsideration and allowance of claims 1-8 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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For Applicant

FDP/tk

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FIG 1

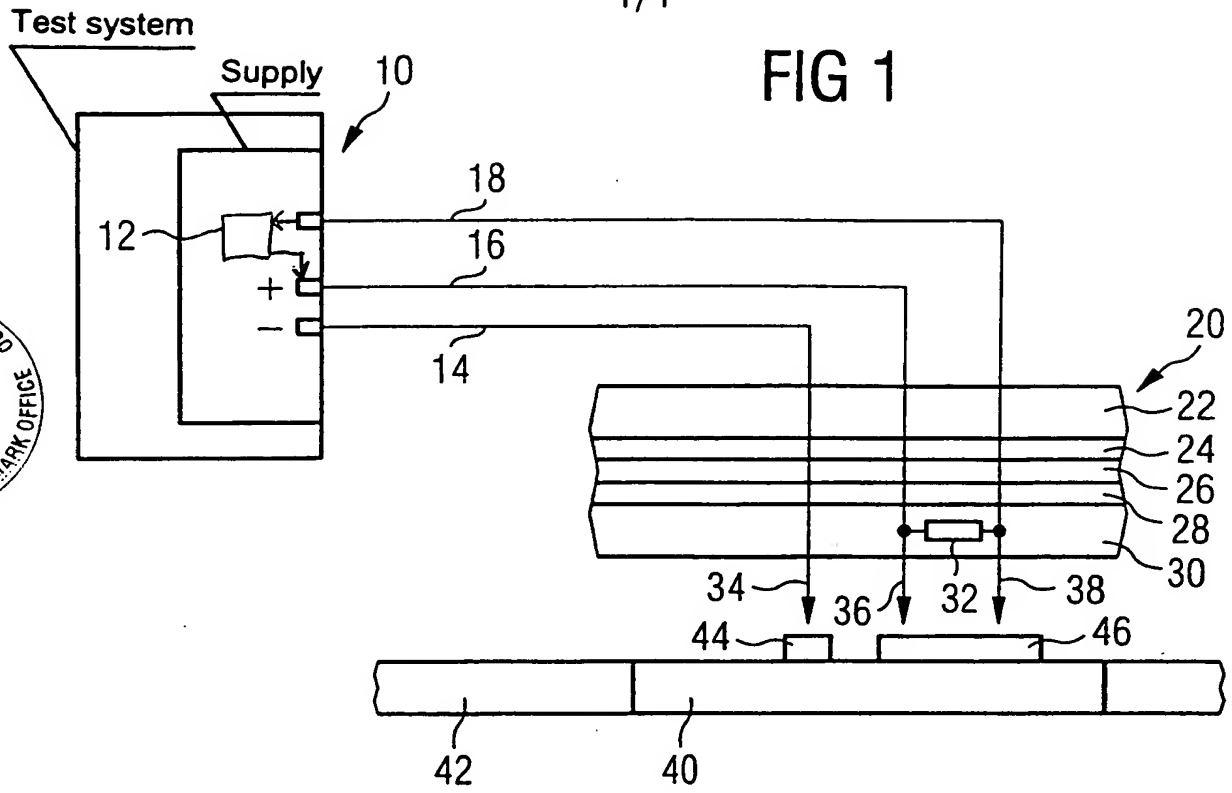

FIG 2